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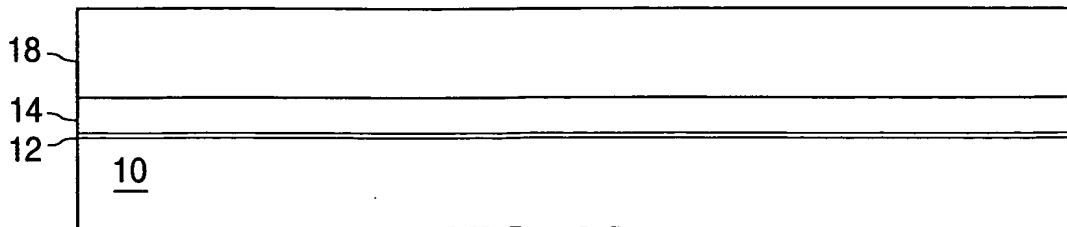


FIG. 1A

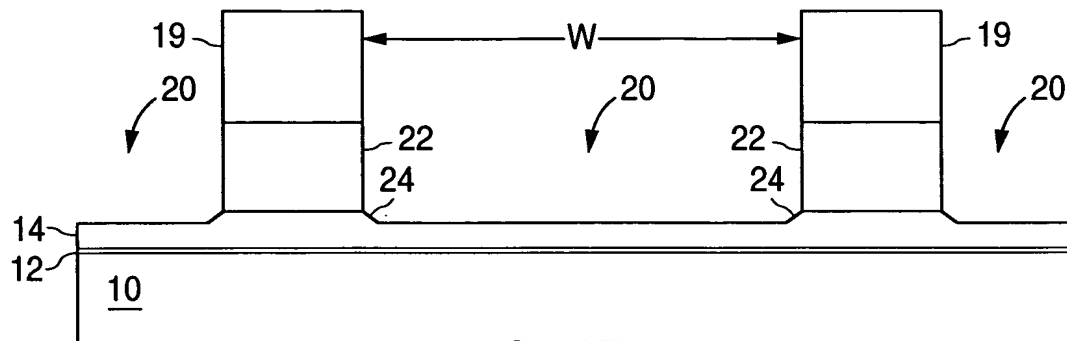


FIG. 1B

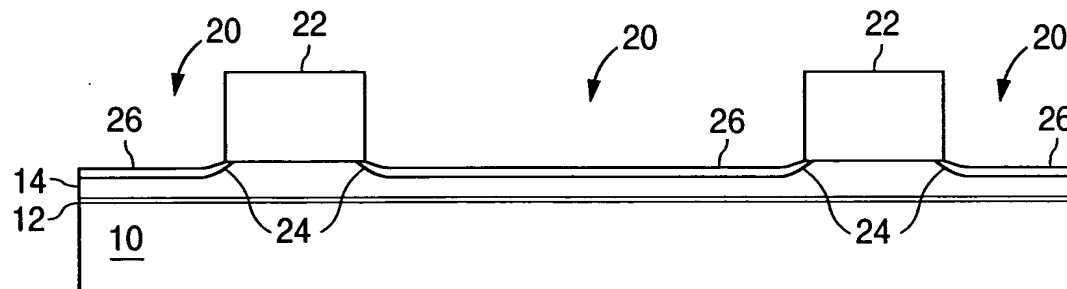


FIG. 1C

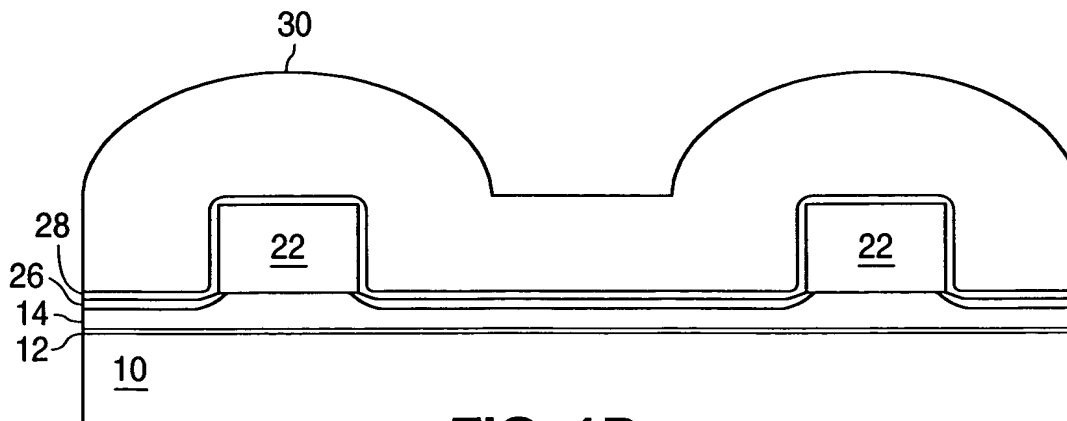


FIG. 1D

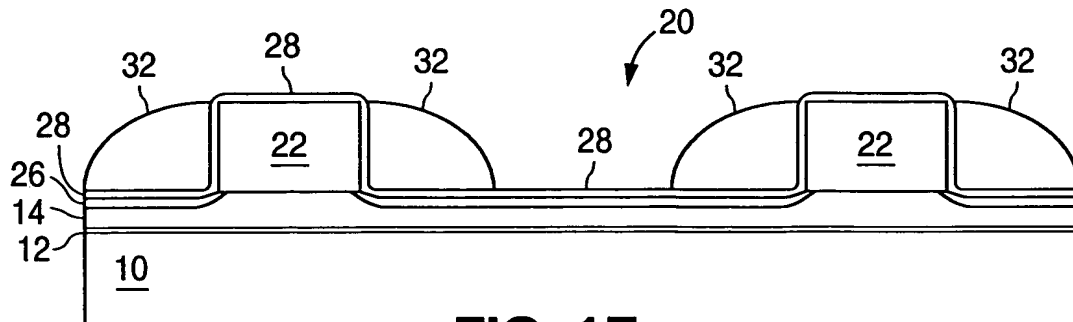


FIG. 1E

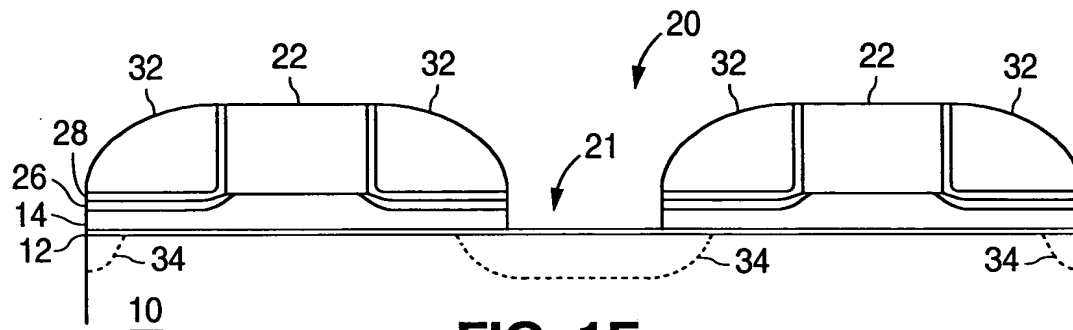


FIG. 1F

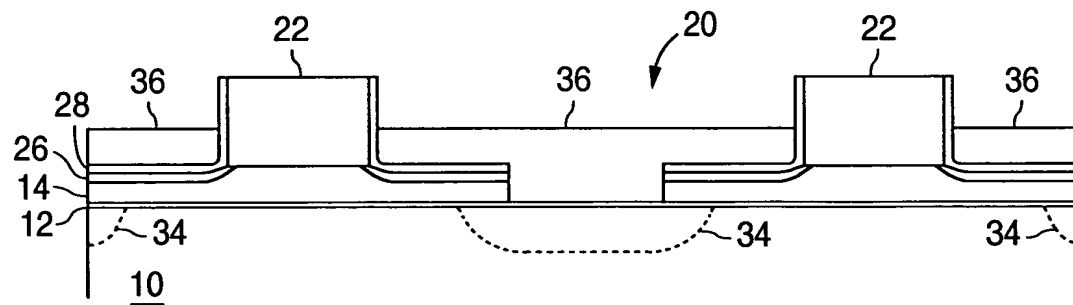


FIG. 1G

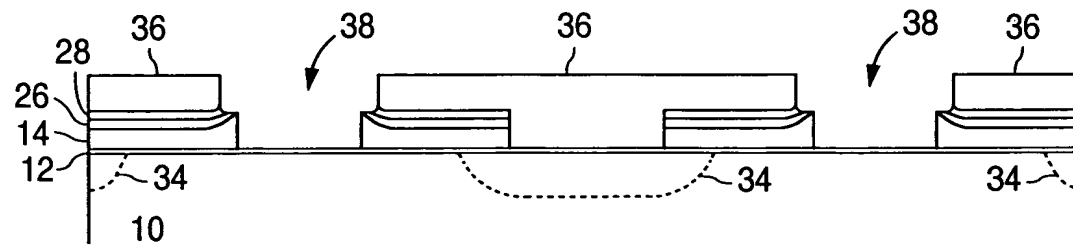
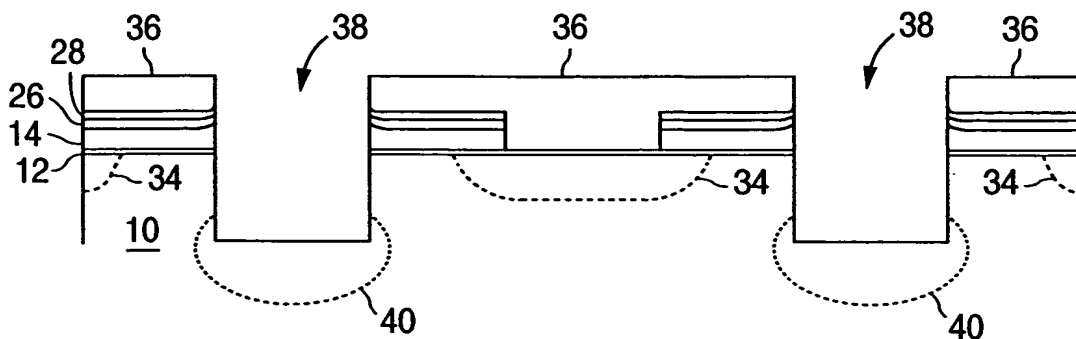
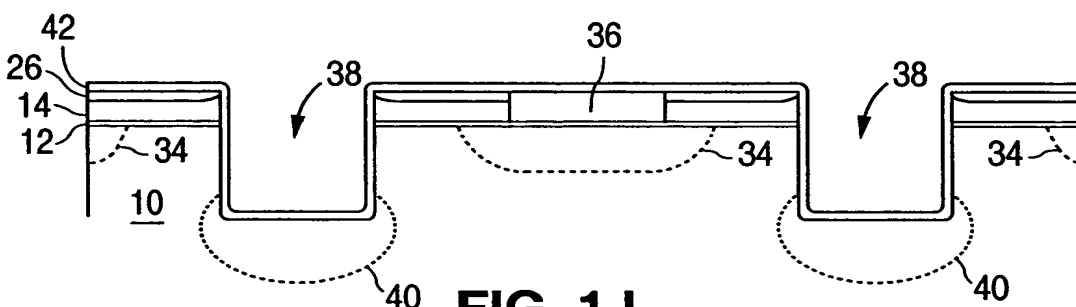


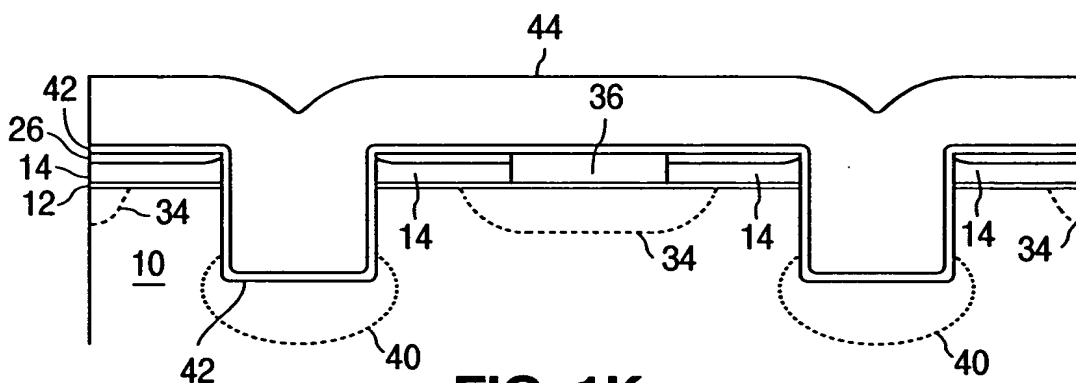
FIG. 1H



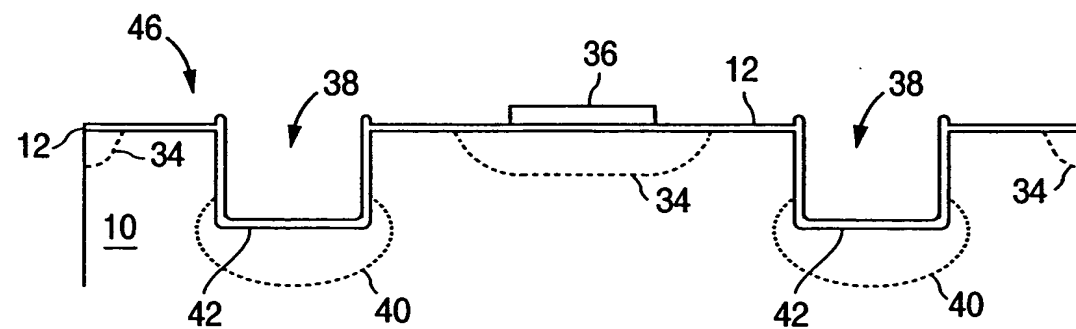
**FIG. 1I**



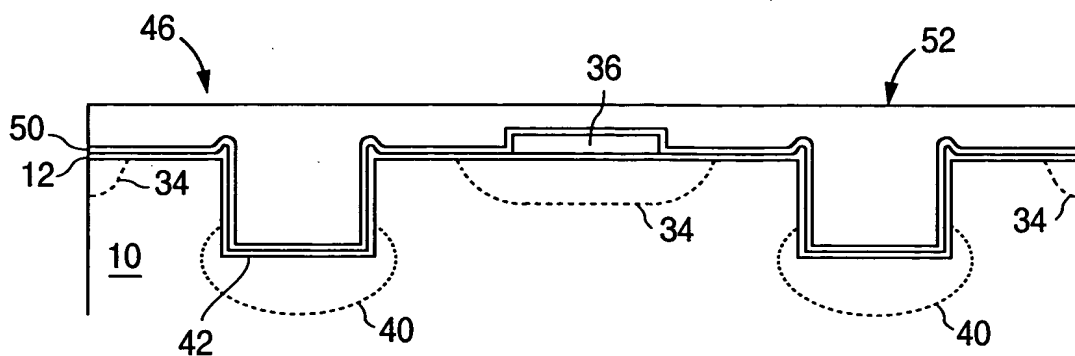
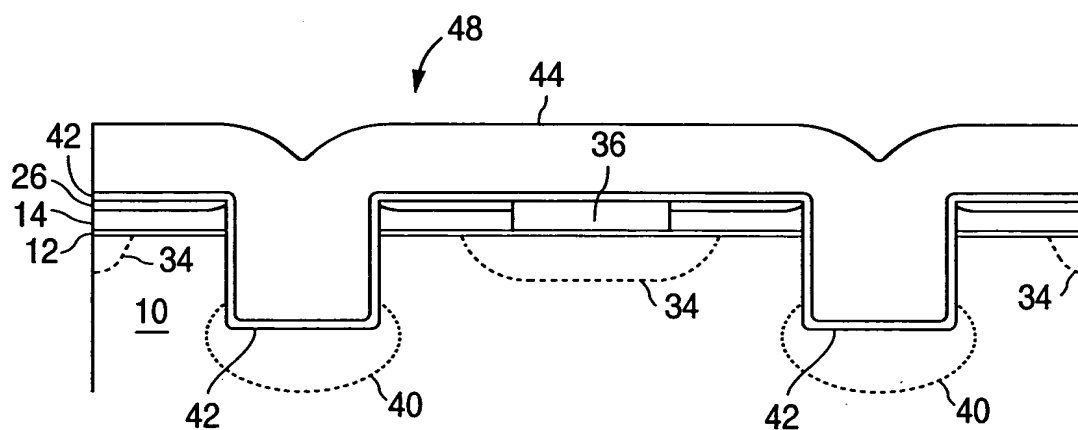
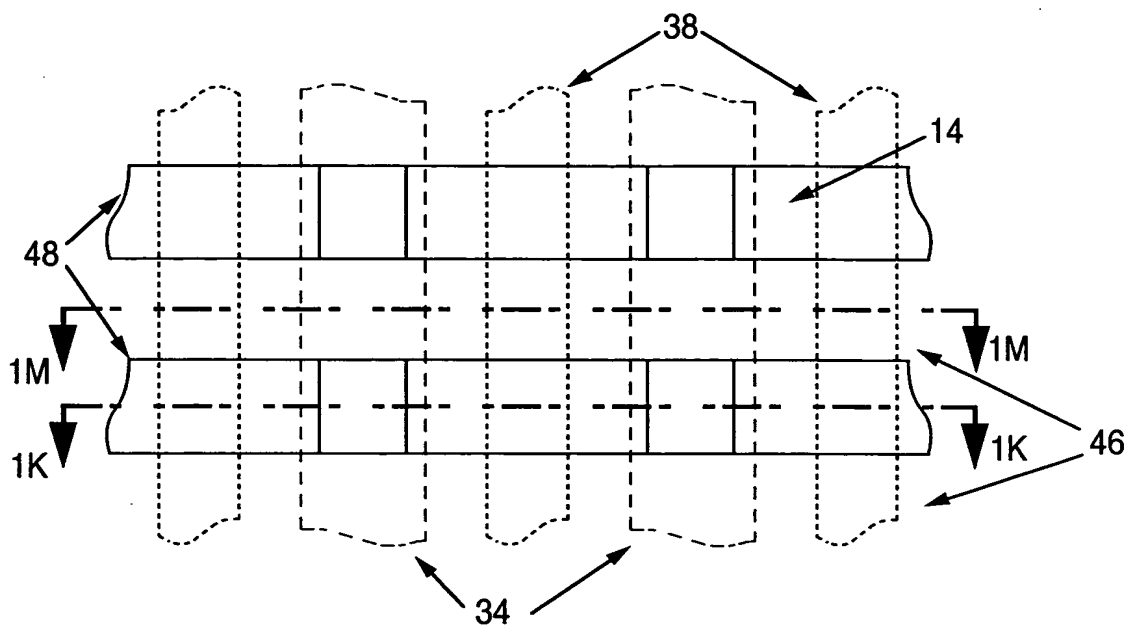
**FIG. 1J**

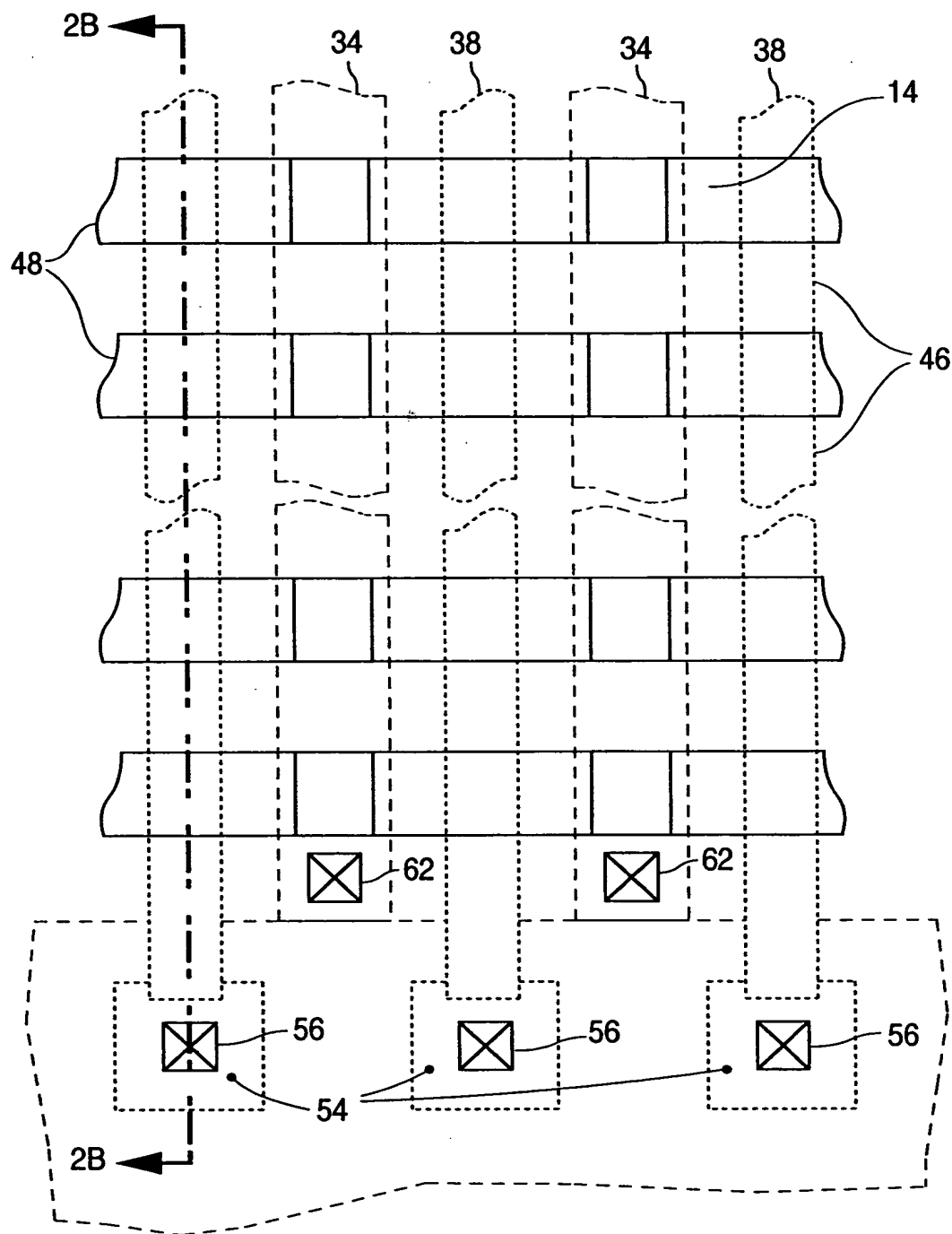


**FIG. 1K**



**FIG. 1M**





**FIG. 2A**

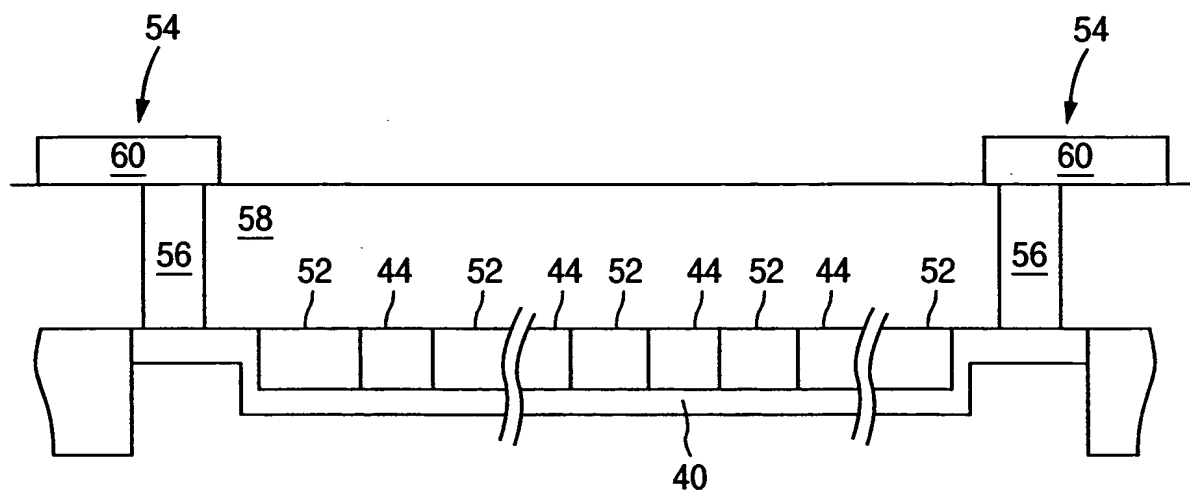
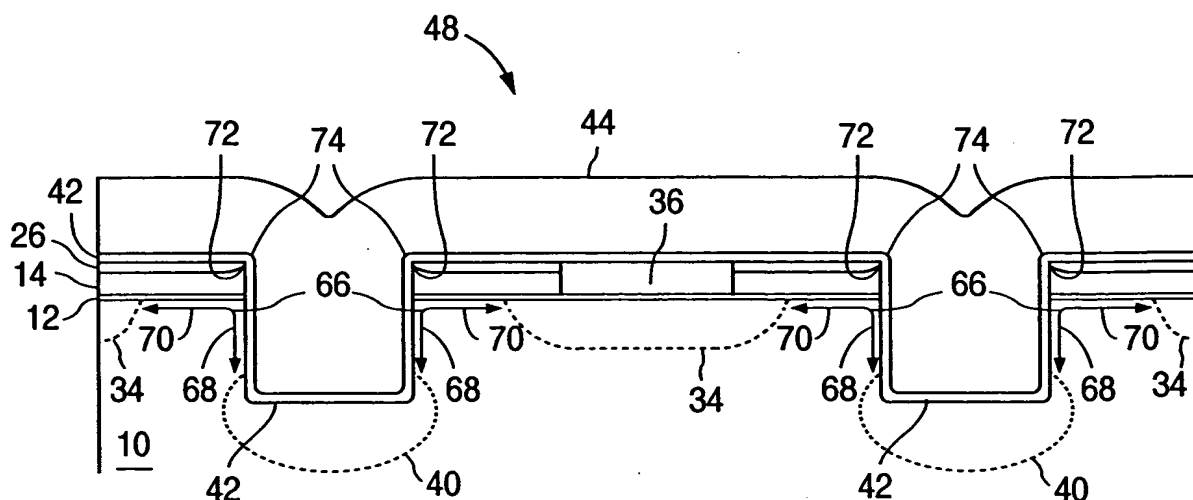
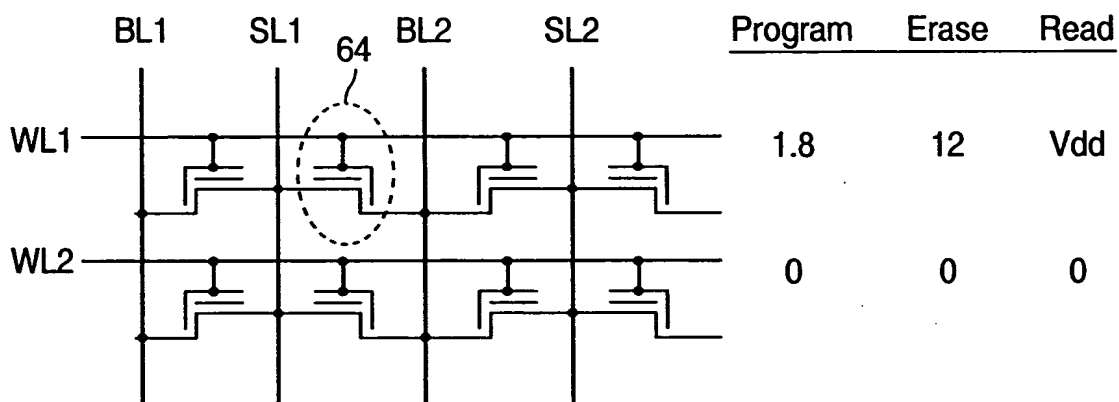


FIG. 3



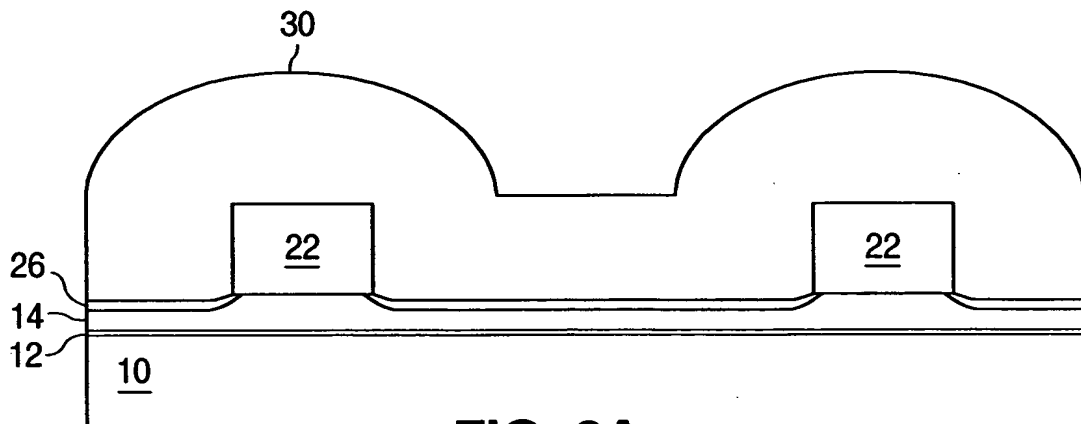
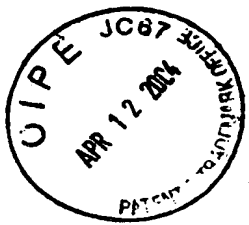
**FIG. 4**



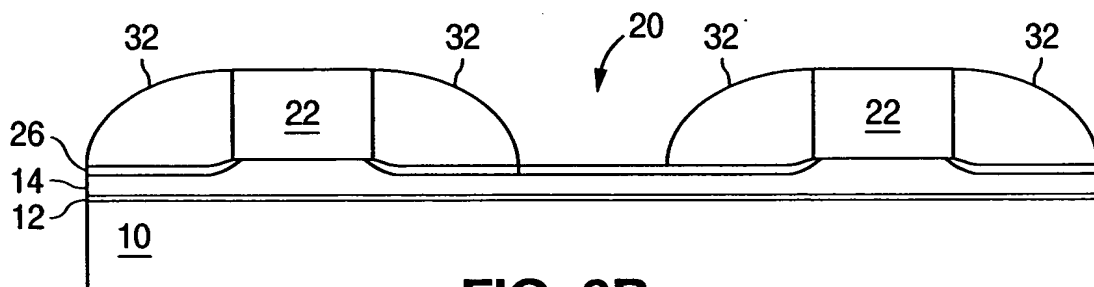
Program	Vdd (inhibit)	Vpp (e.g. 9-10V)	Vdp (0.5-1V)	0 (inhibit)
Erase	0	0	0	0
Read	0	0	~1V	0

**FIG. 5**

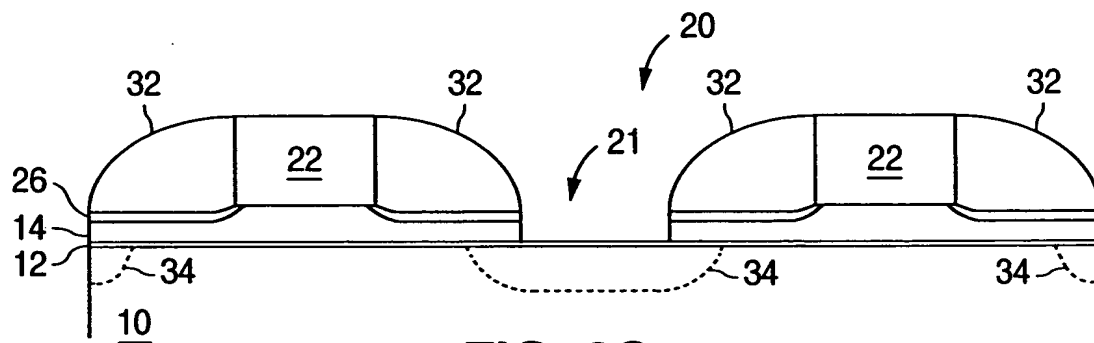




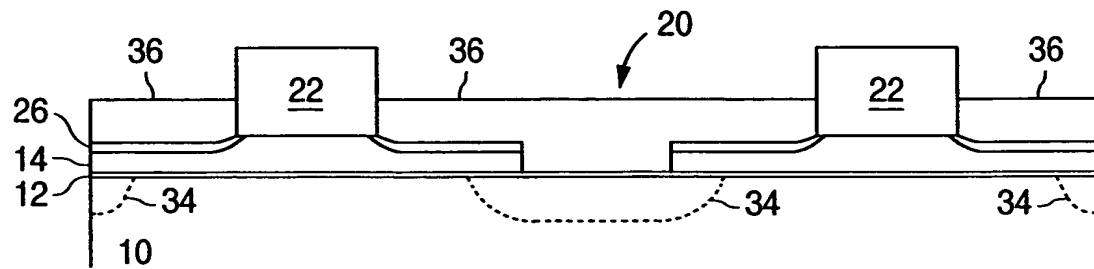
**FIG. 6A**



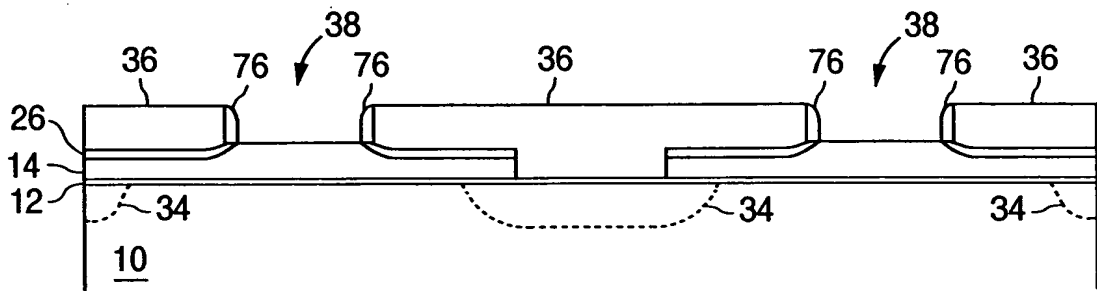
**FIG. 6B**



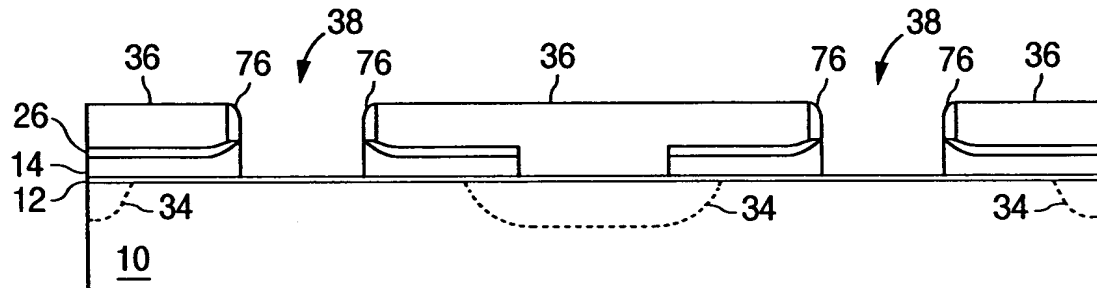
**FIG. 6C**



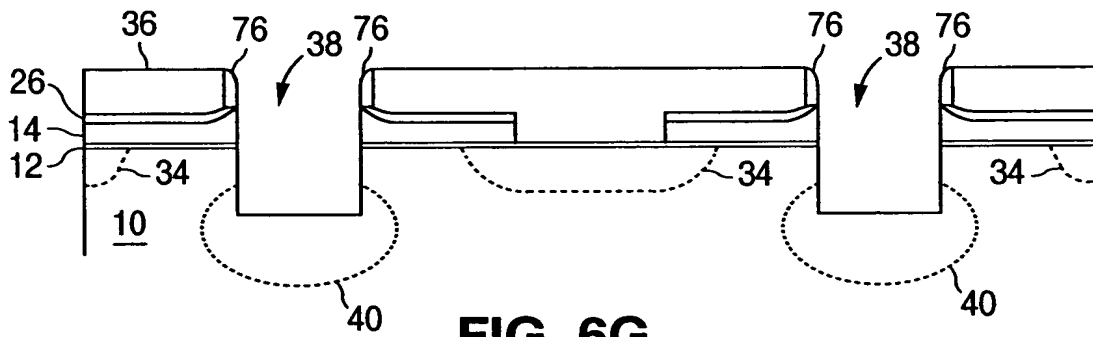
**FIG. 6D**



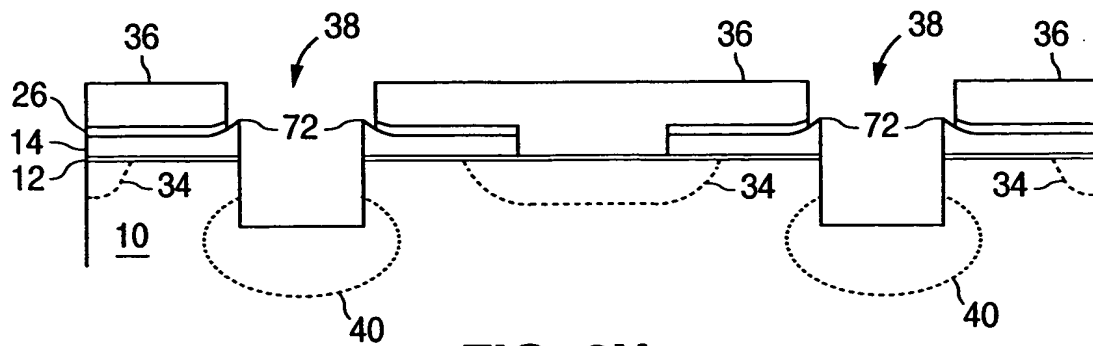
**FIG. 6E**



**FIG. 6F**



**FIG. 6G**



**FIG. 6H**

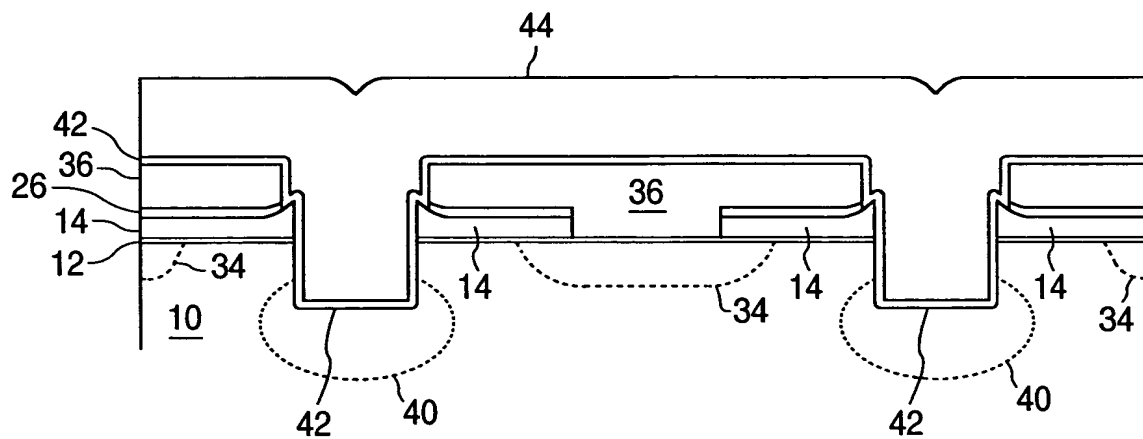
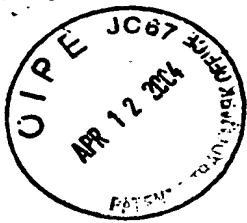


FIG. 6I

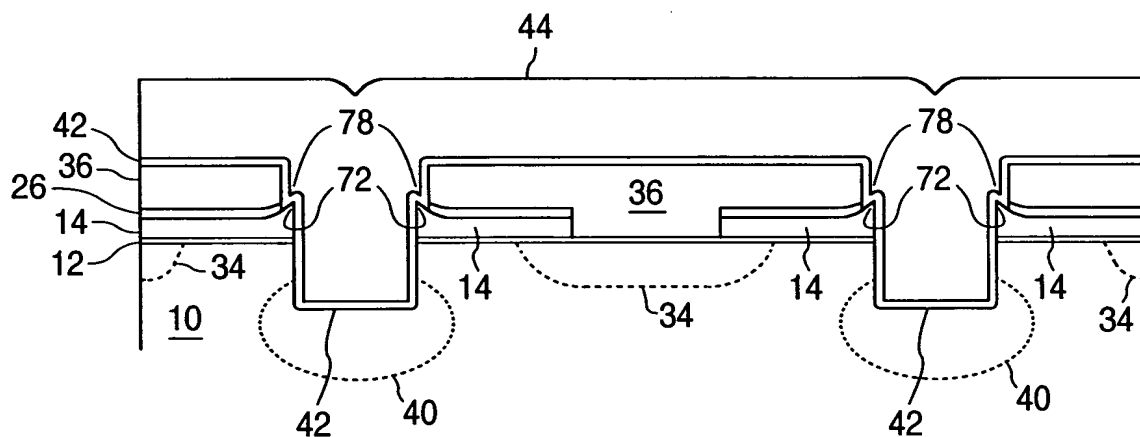


FIG. 6J

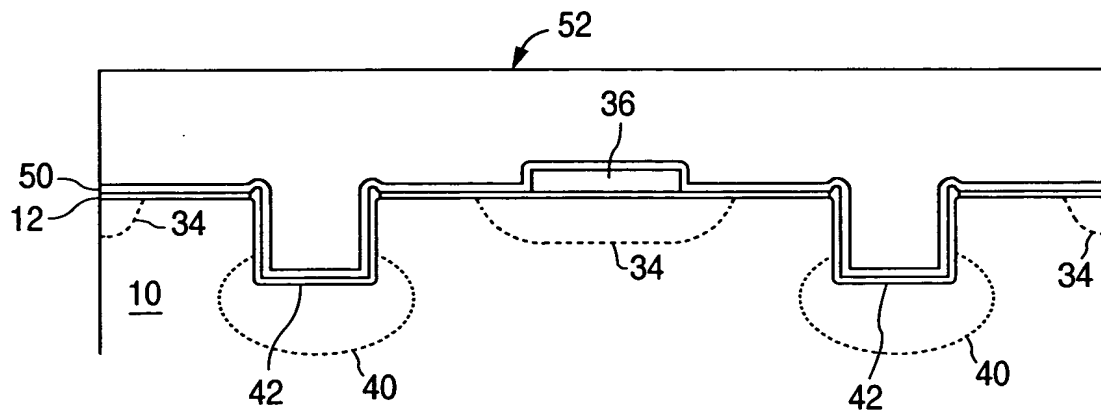


FIG. 6K

